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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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43831	7590	03/08/2006	EXAMINER	
BERKELEY LAW & TECHNOLOGY GROUP			NG, CHRISTINE Y	
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SUITE 240			PAPER NUMBER	
BEAVERTON, OR 97006			2663	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/919,728

Applicant(s)

DENTON ET AL.

Examiner

Christine Ng

Art Unit

2663

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17-24, 27-37 and 46-51 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 17-24 is/are allowed.
- 6) ☒ Claim(s) 27-37 and 46-51 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 33, 27-32 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,515,967 to Wei et al in view of U.S. Patent No. 6,061,725 to Schwaller et al.

Referring to claim 33, Wei discloses a method of testing network communications equipment, comprising:

a) Programming a first set of registers (MRM testers) that define a format of a first test packet (Figure 10). Refer to Column 5, lines 57-64 and Column 11, lines 29-56.

b) Programming a second set of registers (MRM testers) that define a format of second test packet (Figure 10). Refer to Column 5, lines 57-64 and Column 11, lines 29-56.

c) Transmitting a synchronization packet (Figure 7, beacon message). The beacon message is sent by the MRM manager, which is identified by the "synchronization source identifier" (Column 9, lines 7-10).

d) Transmitting the first test packet (Figure 10). Refer to Column 10, lines 25-27.

e) Transmitting, after a first inter-packet gap (Figure 8, interpacket delay 825),

the second test packet (Figure 10). Refer to Column 10, lines 25-27.

Wherein the first test packet (Figure 10) comprises a first packet header (Figure 6), and a first payload (Figure 10); and the second test packet (Figure 10) comprises a second packet header (Figure 6), and a second payload (Figure 10). Refer to Column 7, line 31 to Column 8, line 46 and Column 11, lines 29-56.

Wherein the first and second packet headers (Figure 6) are different. The fields 601-623 of the header in Figure 6 can contain different contents. Refer to Column 7, line 31 to Column 8, line 46.

Wherein further comprising receiving synchronization packet (Column 9, lines 9-14 and lines 26-30), receiving the first test packet, receiving the second test packet; determining if the first test packet was received correctly, and determining if the second test packet was received correctly. Test senders send test packets to test receivers, and test receivers determine whether or not the test packets were received. Test receivers then send a fault report to the MRM manager based on the number of test packets received. Refer to Column 6, lines 21-23; Column 10, line 63 to Column 11, line 6; and Column 11, lines 29-56.

Wei et al do not disclose incrementing a first counter to record the number of received packets.

Schwaller et al disclose a method for monitoring network performance in which there are counters to count the number of packets received, packets transmitted and packets with errors. Refer to Column 1, lines 53-61. Furthermore, Wei et al disclose that one test performed by the MRM manager is to detect packet loss exceeding 20%

over a 10 minute period. This would require that the system count the number of packets transmitted and the number of packets received, so that it can determine a percentage of packets that were not received. Refer to Column 6, lines 21-23.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include incrementing a first counter to record the number of received packets; the motivation being so that the number can be used to determine the number of packets lost or in error, thereby providing a indication of the throughput or efficiency of the system.

Referring to claim 27, Wei et al disclose that the method further comprises, after a second inter-packet gap, transmitting the first test packet. As shown in Figure 2, router 117 is assigned as a test source and routers 113,115 are assigned as test receivers. Therefore, the same consecutive test packets are sent first to one test receiver 113 and then to another test receiver 115. The consecutive test packets are sent according to an interpacket delay as indicated by the MRM manager. Refer to Column 6, lines 53-56 and Column 10, lines 25-37

Referring to claim 28, Wei et al disclose that the method further comprises after a occurrence of the first inter-packet gap, transmitting the second packet. Refer to the rejection of claim 27.

Referring to claims 29 and 30, Wei et al disclose in Figure 10 that the first payload and the second payload can be different or the same. The fields 1003-1017 of the test packet can contain different contents. Refer to Column 11, lines 29-56.

Referring to claims 31 and 32, Wei et al disclose programming the first/second set of registers (MRM testers) comprises writing data into one or more registers so as to define:

1) a total number of bytes (Figure 6, data length 619) in the first/second test packet. Refer to Column 8, lines 1-3.

2) a size of a gap (Figure 8, interpacket delay 825) between the transmission of the first and second test packets. Refer to Column 10, lines 25-27.

3) a pattern (Figure 10) used to fill the first/second payload. Refer to Column 11, lines 29-56.

4) a content of the first/second header (Figure 6). Refer to Column 7, line 31 to Column 8, line 46.

Referring to claim 34, Wei et al do not disclose that the method further comprises incrementing a second counter in response to receipt of a test packet containing an error. Refer to the rejection of claim 33.

Referring to claim 35, Wei et al do not disclose that the method further comprises incrementing a third counter in response to transmission of a test packet by the test generator. Refer to the rejection of claim 33.

Referring to claims 36 and 37, Wei et al do not specifically disclose that transmitting the synchronization packet (Figure 7, beacon message) and receiving the synchronization packet are performed on a single chip [claim 36]; nor that transmitting the synchronization packet is performed on a first integrated circuit chip and receiving the synchronization packet is performed on a second chip [claim 37].

However, Wei et al disclose in Figure 11 a computer system 1100 with a CPU 1102 for performing functions of the disclosed invention, including controlling the reception and manipulation of input data, and the output and display of data on output devices. This includes manipulating the input data, such as the beacon message with the synchronization source identifier. Furthermore, the CPU 1102 can be implemented by a single-chip processor [claim 36] or by multiple processors [claim 37]. Refer to Column 9, lines 9-10 and Column 12, lines 21-36. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that transmitting the synchronization packet and receiving the synchronization packet are performed on a single chip [claim 36]; or that transmitting the synchronization packet is performed on a first integrated circuit chip and receiving the synchronization packet is performed on a second chip [claim 37]. One would be motivated to do so depending on whether the CPU in the system is implemented with a single chip or multiple chips. A single chip simplifies the system and requires less hardware; whereas two chips provides a clear separation of functions.

3. Claims 46-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,228,042 to Gauthier et al in view of U.S. Patent No. 6,515,967 to Wei et al.

Referring to claims 46 and 47, Gauthier et al disclose in Figure 1 a test packet generator comprising:

First test generator logic (LFSR 5) adapted to generate a first (first 10-bit test pattern) and a second (second 10-bit test pattern) test packet.

Transmit logic (data bus 14) adapted to transmit the first test packet and the second test packet.

Receive logic (data bus 22) adapted to receive the first transmitted test packet and the second transmitted test packet, and provide one or more of the first and second transmitted test packets to monitor logic (comparator 60).

Second test generator logic (LFSR 50) adapted to generate a first generated test packet (first 10-bit test pattern) and a second generated test packet (first 10-bit test pattern), and provide one of or more the first and second generated test packets to the monitor logic. A comparator 60 compares the 10-bit test patterns along data bus 22 from LFSR 5 with the 10-bit test patterns generated by LFSR 50. Upon comparison, the comparator generates a true or false signal. A false signal indicates that the 10-bit pattern has been altered during transmission and corrective action must be taken.

Refer to Column 3, line 5 to Column 4, line 2; and Column 4, line 62 to Column 5, line 9.

Gauthier et al do not disclose a synchronization packet; that the first and second test packet have a header and a payload, wherein at least the header of the first packet is different from the header of the second packet; and that the first and the second test packet are transmitted with an inter-packet gap.

Wei et al disclose transmitting a synchronization packet (Figure 7, beacon message, then a first test packet (Figure 10), then a first inter-packet gap (Figure 8, interpacket delay 825), and then a second test packet (Figure 10). Refer to Column 10, lines 25-27 and Column 11, lines 29-56. The first test packet (Figure 10) comprises a first packet header (Figure 6), and a first payload (Figure 10); and the second test

packet (Figure 10) comprises a second packet header (Figure 6), and a second payload (Figure 10); and the first and second packet headers (Figure 6) are different. The fields 601-623 of the header in Figure 6 can contain different contents. Refer to Column 7, line 31 to Column 8, line 46. Refer to the rejection of claim 33. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a synchronization packet; the motivation being to ensure that the transmitting side and receiving side are in sync to facilitate data transmission. One would be motivated to include that the first and second test packet have a header and a payload, wherein at least the header of the first packet is different from the header of the second packet; and that the first and the second test packet are transmitted with an inter-packet gap. One would be motivated to do so in order for the receiver to use the inter-packet delay and different packet headers to distinguish between successive test packet types and perform comparisons accordingly.

Referring to claim 48, Gauthier et al disclose in Figure 1 that the first test generator logic (LFSR 5) and the transmit logic (data bus 14) are implemented on a switch (circuitry) having a plurality of ports (ports X and Y) coupled to a network (switching network 20). Refer to Column 3, lines 24-32.

Referring to claim 49, Gauthier et al disclose in Figure 1 that the receive logic (data bus 22) and the second test generator logic (LFSR 50) are implemented on the switch.

Referring to claim 50, Gauthier et al disclose in Figure 1 that the switch includes a first (port X) and a second (port Y) port, wherein the transmit logic (data bus 14) is

implemented on the first port, and the receive logic (data bus 22) is implemented on the second port.

Referring to claim 51, Gauthier et al disclose in Figure 1 that the monitor logic (comparator 60) is implemented on the switch.

Allowable Subject Matter

4. Claims 17-24 are allowed.

Response to Arguments

5. Applicant's arguments filed December 27, 2005 have been fully considered but they are not persuasive.

Referring to the argument of claim 33 that the beacon messages in Wei et al do not disclose or suggest a synchronization packet (page 7, lines 16-23): Wei et al disclose in Figure 7 a beacon message sent by the MRM manager. The "IP address of MRM manager" field 717 of the beacon message is referred to as a "synchronization source identifier". The MRM manager sending the beacon message is referred to as a "synchronization source" to provide synchronization to the system. Also, the claim does not specify what type of synchronization is provided by the synchronization packet. The beacon message "allows test senders and test receivers to assure the active state of the MRM manager", which is a form of synchronization since all test senders and receivers are in sync as to the state of the MRM manager. Refer to Column 9, lines 7-10 and lines 26-34.

Referring to the argument of claim 33 that Schwaller et al fails to cure the deficiency of Wei et al regarding incrementing a first counter to record the number of

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received packets (page 7, line 24 to page 8, line 10): Wei et al disclose receiving the synchronization packet (Column 9, lines 9-14 and lines 26-30), receiving the first test packet (Figure 10), receiving the second test packet (Figure 10); determining if the first test packet was received correctly, and determining if the second test packet was received correctly. Test senders send test packets to test receivers, and test receivers determine whether or not the test packets were received. Test receivers then send a fault report to the MRM manager based on the number of test packets received. Refer to Column 10, line 63 to Column 11, line 6; and Column 11, lines 29-56. Wei et al do not disclose incrementing a first counter to record the number of received packets. However, a counter is necessary in the system since Wei et al disclose that one test performed by the MRM manager is to detect packet loss exceeding 20% over a 10 minute period. This would require that the system count the number of packets transmitted and the number of packets received, so that it can determine a percentage of packets that were not received. Refer to Column 6, lines 21-23. Schwaller et al disclose a method for monitoring network performance in which there are counters to count the number of packets received, packets transmitted and packets with errors. Refer to Column 1, lines 53-61.

Referring to new claims 46-51, refer to the rejection of claims 46-51.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

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§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

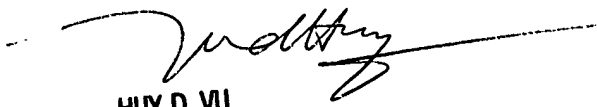
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Ng whose telephone number is (571) 272-3124. The examiner can normally be reached on M-F; 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Ng 
February 27, 2006


HUY D. VU
SUPERVISORY PATENT EXAMINER
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